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(54) Sensor fault detection method and apparatus

(57) An in-range fault detection system for a full wheatstone bridge element 11 2) having piezoresistive elements (R1, R2, R3, R4) has bridge outputs (INP, INM) connected to measuring means in the form of a first circuit portion (13) to provide a common mode voltage (V_{CM}). A second circuit portion (14) is used to provide a centering voltage (C^*V_{BRG}) equal to the common mode voltage at the time of sensor calibration and a third circuit portion (15) is used to provide a small window voltage (W^*V_{BRG}) which is a fraction of bridge voltage. The value (W^*V_{BRG}) is subtracted from (C^*V_{BRG}) at a first summing circuit (SUM1) and added to (C^*V_{BRG}) at a second summing circuit (SUM2) and the results are each compared to the common mode voltage by comparators (Q1, Q2) which are then determined to be within or without a window of valid values by an OR rate (Q3).

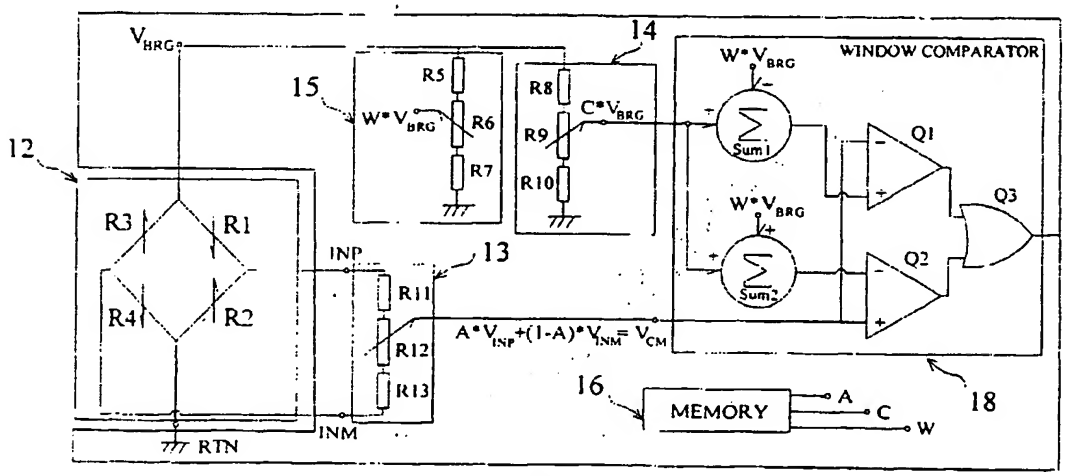

Fig 2

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Description

Field of the Invention

[0001] This invention relates generally to condition responsive sensors having a full bridge circuit such as a bridge circuit comprising piezoresistive elements and more particularly to apparatus and methods for providing fault detection which enables detection of errors in either the offset or sensitivity of a sensor that can be smaller than a full scale output signal.

Background of the Invention

[0002] Bridge circuit sensors are widely used to sense a change in a certain condition, such as a change in pressure or a change in acceleration. A common bridge circuit sensor comprises piezoresistive elements mounted on a substrate, such as silicon, so that changes in the sensed condition causes a change in stress induced in the several piezoresistive elements to provide an output of the bridge which is a function of the change in the sensed condition. Typical uses include acceleration sensors for use in automotive braking systems and pressure sensors for use in automotive fuel injection systems, by way of example. There is a continuing need, in many applications, to minimize costs associated with the sensors while at the same time providing detectivity of sensor flaws which can result in an erroneous in-range sensor output. It is known to use redundant sensors to add to the reliability of a system; however, this adds to the cost of the system. It is desired to provide a single sensor system in which the user is alerted in the event of a malfunction of sensor operation.

[0003] In PCT application, International publication number WO99/01777, dated 14 January 1999, a circuit is disclosed for monitoring the function of a full wheatstone piezoresistive sensor bridge circuit. If the compared signals deviate by more than an acceptable amount the output of a window comparator provides an alarm signal. The disclosed circuit monitors to some extent the bridge resistors as well as the connectivity to an ASIC. However, the cited prior art is complex and is relatively expensive due to its implementation size. The approach in the cited prior art requires two separate conditioning circuits which must be precisely adjusted and stable over time and temperature.

Summary of the Invention

[0004] An object of the present invention is the provision of a method and circuit for detecting faults in a bridge circuit sensor simpler and more cost effective than the above noted prior art. Another object of the invention is the provision of an in-range fault protection system for providing an alarm whenever a fault occurs in a full bridge sensor. Yet another object of the invention is the provision of an in-range fault protection system for a full wheatstone piezoresistive bridge type sensor suitable for fabricating in the form of an integrated circuit which is reliable yet low in cost. Yet another object of the invention is the provision of such a system which can be used for other full bridge arrangements, such as a bridge containing capacitive elements.

[0005] Briefly described, a fault detection system made in accordance with one aspect of the invention comprises circuitry connected to the outputs of an energized full wheatstone bridge to provide a means to generate a common mode voltage of the bridge outputs during sensor calibration which is then compared to a voltage window to determine a fault status during normal operation. The common mode voltage of the full bridge outputs is defined as the voltage equal to a linear combination of the bridge output voltages which is insensitive to stimulus applied to the full bridge and is within the voltage range between the two bridge outputs. Circuit parameters to obtain the common mode voltage and fault window may be appropriately adjusted and stored in nonvolatile memory.

[0006] According to the invention there is provided fault detection apparatus for a full wheatstone bridge comprising a circuit connected between output nodes of the full wheatstone bridge to obtain a common mode voltage signal insensitive to stimulus, a circuit for providing a predetermined voltage window and a circuit for comparing the common mode voltage to a voltage window to determine a sensor fault condition.

[0007] The circuit to yield the common mode voltage signal may be adjustable. Preferably, the circuit to yield the common mode voltage signal comprises a potentiometer resistor string. Alternatively, the circuit to yield the common mode voltage signal comprises at least one adjustable capacitor. The circuit to yield the common mode voltage signal may comprise at least one capacitive Digital-to-Analogue-Converter.

[0008] Preferably, the voltage window is defined by a circuit for adding and subtracting a window width voltage from a window centering voltage where the window centering voltage and window width voltages are proportional to the bridge supply voltage. More preferably, the fault detection apparatus further comprises a circuit for adjusting the window centering voltage in a compensating manner with temperature. The fault detection apparatus may further comprise a circuit for adjusting the window width voltage in a compensating manner with temperature. Preferably, the window width voltage is proportional to the full scale output signal.

[0009] The common mode voltage signal may be an analog signal and the fault detecting apparatus may further comprise a circuit for digitising the analog signal and window parameters and performing calculations in the digital domain on digitised values of the common mode voltage signal and window parameters to determine a fault condition.

[0010] The common mode voltage signal may be derived from a first analog signal, from a first output node of the full wheatstone bridge, and from a second analog signal, from a second output node of the full wheatstone bridge, and the fault detection apparatus may further comprise a circuit for digitising the first analog signal, a circuit for digitising the second analog signal, a circuit for digistising parameters of the voltage window and a circuit for performing calculations in the digital domain on digitised values of the first analog signal and the second analog signal to form the common mode voltage signal and on the common mode voltage signal and digitised values of the window parameters to determine a fault condition.

[0011] Preferably, the full wheatstone bridge comprises piezoresistive elements. Also according to the invention there is provided a method for monitoring faults of a full wheatstone bridge sensor element and connections thereto, the sensor elements having bridge outputs, comprising the steps of:

energising the bridge sensor element with a power source,
adjusting a circuit between the outputs of the full wheatstone bridge sensor element to yield a common mode voltage signal, which is equal to a linear combination of the bridge output voltages and is insensitive to stimulus during sensor calibration,
storing the adjusted circuit parameters in memory for setting the common mode voltage,
comparing the common mode voltage to a fault window; and
setting a fault indication whenever the common mode voltage exceeds the fault window.

[0012] Preferably, the fault window is defined by a voltage range defined by a window centering voltage and a window width voltage which are both proportional to the bridge supply voltage. Preferably, the window centering voltage is equal to the common mode voltage at the time of sensor calibration. Preferably, the fault window is defined between the window centering voltage minus the window width voltage to the window centering voltage plus the window width voltage.

[0013] Preferably, the window width voltage is proportional to the full scale output of the full wheatstone bridge.

[0014] Preferably, the common mode voltage is fixed to equal the average of the bridge output voltages.

[0015] Preferably, the bridge sensor element is supplied with a voltage source. Preferably, the bridge sensor element is supplied with a voltage source through a series resistor. Alternatively, the bridge sensor element may be supplied with a current source.

Brief Description of the Drawings

[0016] Other objects, advantages and details of the sensor of the invention and method for providing in-range fault detection appear in the following detailed description of preferred embodiments of the invention, the detailed description referring to the following drawings in which:

Fig. 1 is a schematic of a full wheatstone bridge sensor element and an ASIC embodying a circuit made in accordance with the invention;

Fig. 2 is a schematic of the common mode fault detection circuit portion of the Fig. 1 ASIC showing circuit portions for providing common mode voltage, window centering voltage and window width voltage, and a window comparator circuit;

Fig. 2a is a schematic of a modification of the Fig. 2 structure which includes a temperature compensation circuit for the common mode voltage, window centering voltage and window width voltage;

Fig. 2b is a schematic of the common mode voltage circuit portion of the common mode fault detection circuit portion of Fig. 2 showing an alternate embodiment of the invention using capacitive DACs for obtaining the common mode voltage;

Fig. 2c is a schematic similar to Fig. 2a of a modified embodiment employing analog to digital converters to perform calculations in the digital domain;

Fig. 3 is a schematic of a portion of the Fig. 1 ASIC showing the full bridge sensor element power source as a voltage source;

Fig. 3a is a schematic similar to Fig. 3 showing the full bridge sensor element power source as a voltage source and a series resistor; and

Fig. 3b is a schematic similar to Fig. 3 showing the full bridge sensor element power source as a current source.

Detailed Description of the Preferred Embodiment

[0017] With reference to Fig. 1, a piezoresistive sensor conditioner application specific, integrated circuit (ASIC) 10 is shown along with a piezoresistive sensor element 12 made in accordance with a preferred embodiment of the invention. ASIC 10 will convert small changes in the off-chip piezoresistors of sensor element 12 to large changes in the ASIC supply-ratiometric output voltage. Four piezoresistors R1-R4 are arranged in a full wheatstone bridge, in externally connected sensing element 12. The value of resistors R1-R4 vary in response to the application of a mechanical stimulus such as pressure used in various applications including automotive under-hood applications such as fuel injection systems. ASIC 10 has nodes BRG, INP, INM, and RTN for connection to nodes of sensor element 12 in turn connected to resistors R1-R4 of sensor element 12 as well as nodes PWR, OUT, and RTN for external connection of power and the sensor output.

[0018] In accordance with the preferred embodiment of the invention, common mode voltage, V_{CM}, is obtained using a circuit portion 13 connected between the bridge voltage output connections INP, INM. As will be explained in greater detail below, voltage V_{CM} is equal to $A^*V_{INP}+(1-A)^*V_{INM}$. In the Fig. 2 embodiment, circuit portion 13 comprises a first DAC made up of resistors R11, R12 and R13. A fault windowing centering voltage, C^*V_{BRG}, is obtained using a circuit portion 14 in the form of a second DAC made up of resistors R8, R9 and R10 and a fault parameter window width parameter, W^*V_{BRG}, is obtained using a third circuit portion 15 in the form of a third DAC made up of resistors R5, R6 and R7. The values of A, C and W are stored in nonvolatile memory 16. The output of circuit portions 13, 14 and 15 are connected to window comparator 18, to be discussed below, in order to obtain an indication of the status of a fault condition.

[0019] The fault detection system is calibrated by first adjusting the common mode voltage, V_{CM} to be insensitive to applied stimulus to the full bridge equal to a linear combination of the full bridge output voltages V_{INP}, V_{INM} bounded by the full bridge output voltages (i.e., $V_{CM} = \{A\ V_{INP} + (1\text{-}A)\ V_{INM}\}$, where $0 < A < 1$ and $V_{CM} \neq f(\text{stimulus})$). Perfect matching of the stimulus sensitivities of the two half bridges results in the common mode voltage being equal to the average of the two half bridge outputs (i.e., $V_{CM} = (V_{INP} + V_{INM})/2$; $A = 0.50$).

[0020] Fault window centering voltage, C^*V_{BRG}, proportional to the bridge supply voltage V_{BRG}, is adjusted to be nearly equal to the common mode voltage V_{CM} following common mode voltage trimming.

[0021] Fault window width parameter W^*V_{BRG} is adjusted to equal a known fraction of the bridge supply voltage. Alternatively, if desired, the fault window width parameter can be made equal to a known fraction of the full scale output. The window width parameter, W is typically adjusted to be as small as possible to maximize fault detectivity. In order to avoid false fault reporting over time, temperature, and the like, the lower limit of the window width parameter is selected to be sufficiently larger than the expected variations in common mode voltage not compensated for during sensor calibration as well as ASIC influences such as calibration error and drift.

[0022] Calibration adjustments requiring thermal compensation involve repeating the calibration process at multiple temperatures to set linear and higher order thermal coefficients of compensation. All adjustable parameters are stored in nonvolatile memory 16. Sensors requiring thermal compensation may derive a temperature signal either from a conventional temperature reference on the ASIC 10 as indicated in Fig. 2a, to be discussed, (e.g., a signal related to a bandgap reference voltage) or by a signal related to the sense element temperature. One method to obtain a signal related to the sensor element temperature is to power the sensor element as shown in either Figs. 3a or 3b and use the temperature variation in V_{BRG}, due to the sensor bridge resistance temperature dependence, as the temperature signal. As shown in figure 3a, a series resistance, R_{SERIES} is provided having significantly lower thermal variation than the full bridge resistance would cause the bridge voltage V_{BRG} to vary over temperature mainly due to the resistance change in the full bridge resistance. Similarly, as shown in figure 3b, a current source, I_{SOURCE} is provided having significantly lower thermal variation than the full bridge resistance would cause the bridge voltage, V_{BRG} to vary over temperature mainly due to the full bridge resistance thermal variation. However, the bridge powering techniques shown in figures 3a and 3b reduce the sensor element 12 signal by the fraction of V_{BRG}/V_{PWR}. Embodiments not deriving the temperature signal from the sensor element may employ the bridge powering technique shown in figure 3 to maximize sensor signal thereby reducing required ASIC gain.

[0023] As noted above, during operation of a calibrated fault detection system made in accordance with a preferred embodiment of the invention, the common mode voltage of the two bridge halves is obtained at circuit portion 13 comprising an adjustable resistor divider tap or first potentiometric DAC output which is serially connected between the bridge output nodes. The setting, A of the first DAC having an output $V_{CM} = \{A^*V_{INP} + (1\text{-}A)^*\ V_{INM}\}$ is selected such that the common mode voltage is insensitive to applied stimulus to the full bridge. Circuit portion 14 comprising the

second DAC connected between the bridge voltage V_{BRG} and analog ground V_{RTN}, is adjusted to center the fault window and satisfy the relation $V_C \sim V_{CM}$. Circuit portion 15 comprising the third DAC, connected between the bridge voltage and analog ground, is set to yield half the fault window width. The parameter $W*V_{BRG}$ is then added to $C*V_{BRG}$ at a first summing circuit SUM1 and in turn inputted to the positive input of the first comparator Q1 and subtracted from $C*V_{BRG}$ at a second summing circuit SUM2 and in turn inputted to the negative input of the second comparator Q2. The outputs of the comparators Q1and Q2 are connected to the inputs of a digital logic OR gate Q3 so that if the common mode voltage falls outside the window bounded by $(C - W)*V_{BRG}$ to $(C + W)*V_{BRG}$ a fault is indicated by a logic "1" output of the OR gate Q3. The output of the OR gate Q3 reflects the status of the fault condition so that the user is alerted to a malfunction of the sensor element or its connectivity to the ASIC.

[0024] The above embodiment may be further simplified by eliminating certain ASIC adjustments to the common mode fault parameters by carefully controlling or screening bridge parameters which influence the stimulus, time and temperature variability of the bridge common mode voltage. For example, the resistive DAC of circuit portion 13 used to yield the common mode voltage may be replaced by a pair of equal valued resistors (not shown) between the full bridge outputs if the stimulus sensitivities of the two half bridges are matched sufficiently well.

[0025] Alternatively, as shown in Fig. 2b, circuit portion 13 can comprise first and second capacitive DACs C11, C12 coupled to a comparator Q4 to provide common mode voltage V_{CM}.

[0026] With reference to Fig. 2a, a modified embodiment includes thermal compensation provided by temperature conditioning circuit 20 in which A is equal to A0+1*(T-T0)/T0+A2*[(T-T0)/T0]^2 +...An* [(T-T0/T0]^n; C=C0+C1*(T-T0)/T0+C2*[T-T0)/T0]^2+...(m[T-T0)/T0]^m; and W=W0+W1*(T-T0)/T0+W2*[T-T0/T0)T0]^ 2+...+Wp*[(T-T0)/T0]^p. Memory 16 has ports n - A0, A1, A2,...An; m - C0, C1, C2...Cm; p - W0, W1, W2,...Wp interconnected with temperature conditioning circuit 20. Thermal compensation for the window centering voltage may be eliminated by careful control of sense element parameters which affect the common mode voltage over temperature.

[0027] Although a fraction of the bridge supply voltage has been used to provide the centering voltage and the windowing values, as noted above, it is within the purview of the invention to derive the window width values from the full scale span. Thus, the window width voltage may be inversely proportional to ASIC gain. During sensor calibration, the thermal compensation coefficients for the window width parameter may be functionally related to the sensor's stimulus gain thermal compensation coefficients, thereby providing a window setting given by a known fraction of full scale output over a defined temperature range.

[0028] In another modified embodiment, digitized analog signals related to the full bridge output and supply voltages can be employed. The digitized data are then evaluated to determine the presence of a fault condition caused by changes in the common mode voltage of the full bridge. With reference to Fig. 2c, conditioning circuit 22 and analog to digital converter 24, connected between voltage V_{BRG} and common, are connected to voltage V_{BRG} and provide a digitized signal at X which is inputted to microcontroller 34. Conditioning circuit 26 and analog to digital converter 28, connected between voltage V_{BRG} and common, are connected to voltage V_{INP} and provide a digitized signal at Y which is inputted to microcontroller 34. Similarly, conditioning circuit 30 and analog to digital converter 32, connected between voltage V_{BRG} and common, are connected to voltage V_{INM} and provide a digitized signal at Z which is inputted to microcontroller 34. The microcontroller performs calculations based on the inputs from X, Y and Z along with values from memory 16: n - A0, A1, A2,...An; m - C0, C1, C2,...Cm; p - W0, W1, W2...Wp according to the following:

$$A = A0+A1*(T-T0)/T0+A2*[(T-T0)/T0]^2+...+An*\{(T-T0)/T0]^n$$

$$C = C0+C1*(T-T0)/T0+C2*\{(T-T0)/T0]^2+...Cm*[(T-T0)/T0]^m$$

$$W = W0+W1*(T-T0)/T0+W2*[(T-T0)/T0]^2+...+Wp*[(T-T0)/T0]^p$$

$$\text{IF } \{A*Y+(1-A)*Z\} > (C + W)*X \text{ THEN FAULT} = 1$$

$$\text{IF } \{A*Y+(1-A)*Z\} < (C - W)*X \text{ THEN FAULT} = 1$$

[0029] It is within the scope of the invention, as shown in figure 2b that capacitive dividers and capacitive DACs may be used to generate the necessary signals related to the full bridge voltages. One method to provide generation of the V_{CM} signal using a pair of capacitive DACs comprises hardware and clocking as follows; simultaneously close a pair of switches S1 and S2, while switches S3 and S4 are open, with a clock signal θ1 to store the bridge output voltages

V_{INP} and V_{INM} on adjustable capacitors C11 and C12, respectively. Following the settling of the voltages on adjustable capacitors C11 and C12, clock phase θ1 opens switches S1 and S2 between the bridge and capacitors and a brief period later clock signal θ2 simultaneously closes a pair of switches, S3 and S4 to store V_{CM} onto a sample and hold circuit given by a capacitor C13 and an amplifier Q4 in a buffer feedback configuration The value of capacitor C13 with respect to adjustable capacitors C11 and C12 influences circuit response time. The adjustable capacitors C11 and C12 should be adjusted to yield V_{CM} which is insensitive to stimulus applied to the bridge. If desired, only one of C11 or C12 needs to be made adjustable to accommodate the required V_{CM} trimming. Also, it is obvious and within the purview of the invention to employ a non-unity gain to the amplifier Q4.

[0030] It should be understood that although a particular embodiment of the invention has been described by way of illustrating the invention, the invention includes all modifications and equivalents of the disclosed embodiment falling within the scope of the appended claims.

Claims

1. Fault detection apparatus for a full wheatstone bridge comprising a circuit connected between output nodes of the full wheatstone bridge to obtain a common mode voltage signal insensitive to stimulus, a circuit for providing a predetermined voltage window and a circuit for comparing the common mode voltage to a voltage window to determine a sensor fault condition.

2. Fault detection apparatus according to claim 1, in which the circuit to yield the common mode voltage signal is adjustable.

3. Fault detection apparatus according to claim 2, in which the circuit to yield the common mode voltage signal comprises a potentiometer resistor string.

4. Fault detection apparatus according to claim 2, in which the circuit to yield the common mode voltage signal comprises at least one adjustable capacitor.

5. Fault detection apparatus according to claim 4, in which the circuit to yield the common mode voltage signal comprises at least one capacitive Digital-to-Analogue - Converter.

6. Fault detection apparatus according to any preceding claim, in which the voltage window is defined by a circuit for adding and subtracting a window width voltage from a window centering voltage where the window centering voltage and window width voltages are proportional to the bridge supply voltage.

7. Fault detection apparatus according to claim 6, further comprising a circuit for adjusting the window centering voltage in a compensating manner with temperature.

8. Fault detection apparatus according to claim 6 or claim 7, further comprising a circuit for adjusting the window width voltage in a compensating manner with temperature.

9. Fault detection apparatus according to any of claims 5 to 8, in which the window width voltage is proportional to the full scale output signal.

10. Fault detection apparatus according to any preceding claim, in which the common mode voltage signal is an analog signal and further comprising a circuit for digitising the analog signal and window parameters and performing calculations in the digital domain on digitised values of the common mode voltage signal and window parameters to determine a fault condition.

11. Fault detection apparatus according to any of claims 1 to 9, in which the common mode voltage signal is derived from a first analog signal, from a first output node of the full wheatstone bridge, and from a second analog signal, from a second output node of the full wheatstone bridge, and further comprising a circuit for digitising the first analog signal, a circuit for digitising the second analog signal, a circuit for digitising parameters of the voltage window and a circuit for performing calculations in the digital domain on digitised values of the first analog signal and the second analog signal to form the common mode voltage signal and on the common mode voltage signal and digitised values of the window parameters to determine a fault condition.

12. Fault detection apparatus according to any preceding claim, in which the full wheatstone bridge comprises piezoresistive elements.

13. A method for monitoring faults of a full wheatstone bridge sensor element and connections thereto, the sensor elements having bridge outputs, comprising the steps of:

energising the bridge sensor element with a power source,
adjusting a circuit between the outputs of the full wheatstone bridge sensor element to yield a common mode voltage signal, which is equal to a linear combination of the bridge output voltages and is insensitive to stimulus during sensor calibration,
storing the adjusted circuit parameters in memory for setting the common mode voltage,
comparing the common mode voltage to a fault window; and
setting a fault indication whenever the common mode voltage exceeds the fault window.

14. A method according to claim 13, in which the fault window is defined by a voltage range defined by a window centering voltage and a window width voltage which are both proportional to the bridge supply voltage.

15. A method according to claim 14, in which the window centering voltage is equal to the common mode voltage at the time of sensor calibration.

16. A method according to claim 14 or claim 15, in which the fault window is defined between the window centering voltage minus the window width voltage to the window centering voltage plus the window width voltage.

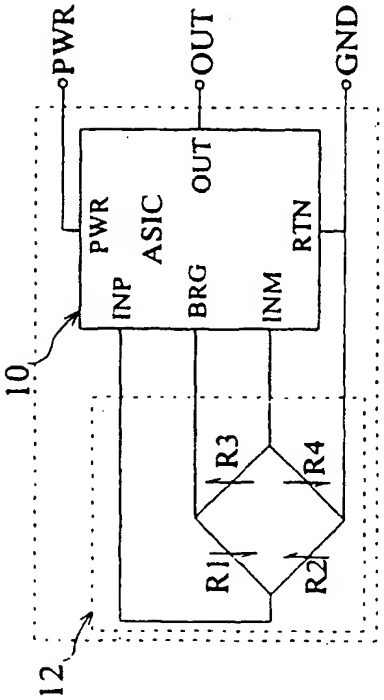
17. A method according to any of claims 14 to 16, in which the window width voltage is proportional to the full scale output of the full wheatstone bridge.

18. A method according to any of claims 13 to 17, in which the common mode voltage is fixed to equal the average of the bridge output voltages.

19. A method according to any of claims 13 to 18, in which the bridge sensor element is supplied with a voltage source.

20. A method according to claim 19, in which the bridge sensor element is supplied with a voltage source through a series resistor.

21. A method according to any of claims 13 to 18, in which the bridge sensor element is supplied with a current source.


PWR
OUT
GND
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PWR
ASIC
OUT
INP
BRG
INM
RTN
R3
R4
R1
R2
12

Fig 1

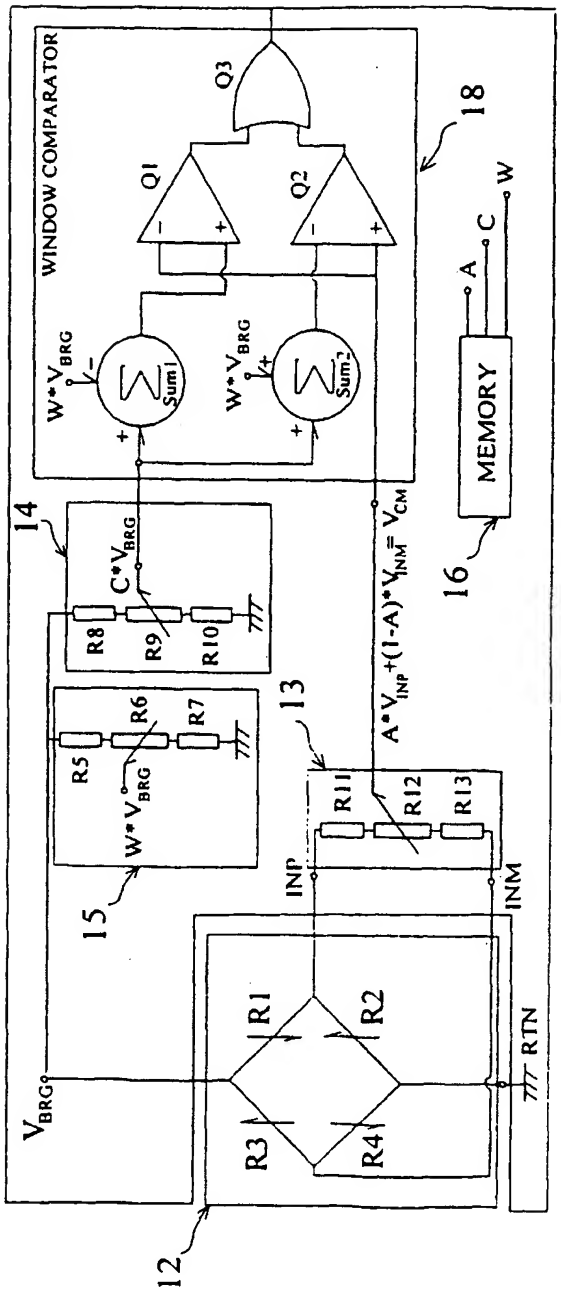
WINDOW COMPARATOR
Q3
Q1
Q2
18
W
C
A
W*V_BRG
Sum1
W*V_BRG
Sum2
MEMORY
16
14
C*V_BRG
R8
R9
R10
13
R6
R7
R5
W*V_BRG
15
A*V_INP+(1-A)*V_INM= V_CM
R11
R12
R13
INP
INM
V_BRG
R1
R2
R3
R4
RTN
12

Fig 2

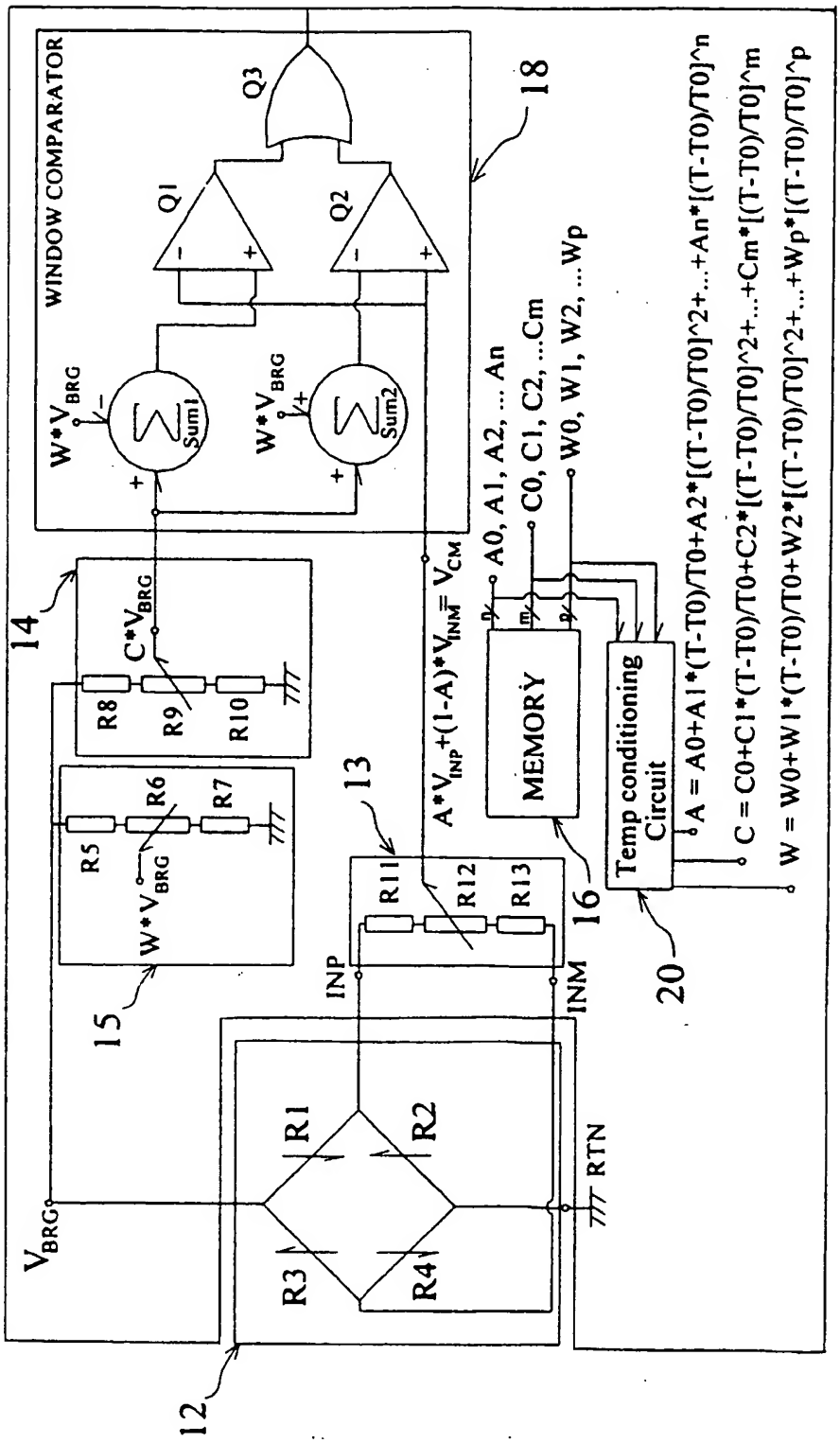
WINDOW COMPARATOR
Q1
Q2
Q3
18
W*V_BRG
Sum1
W*V_BRG
Sum2
14
C*V_BRG
R8
R9
R10
R5
R6
R7
W*V_BRG
15
13
R11
R12
R13
A*V_INP+(1-A)*V_INM= V_CM
MEMORY
16
A0, A1, A2, ... An
C0, C1, C2, ...Cm
W0, W1, W2, ...Wp
Temp conditioning Circuit
20
A = A0+A1*(T-T0)/T0+A2*[(T-T0)/T0]^2+...+An*[(T-T0)/T0]^n
C = C0+C1*(T-T0)/T0+C2*[(T-T0)/T0]^2+...+Cm*[(T-T0)/T0]^m
W = W0+W1*(T-T0)/T0+W2*[(T-T0)/T0]^2+...+Wp*[(T-T0)/T0]^p
INP
INM
R1
R2
R3
R4
RTN
V_BRG
12

Fig 2a

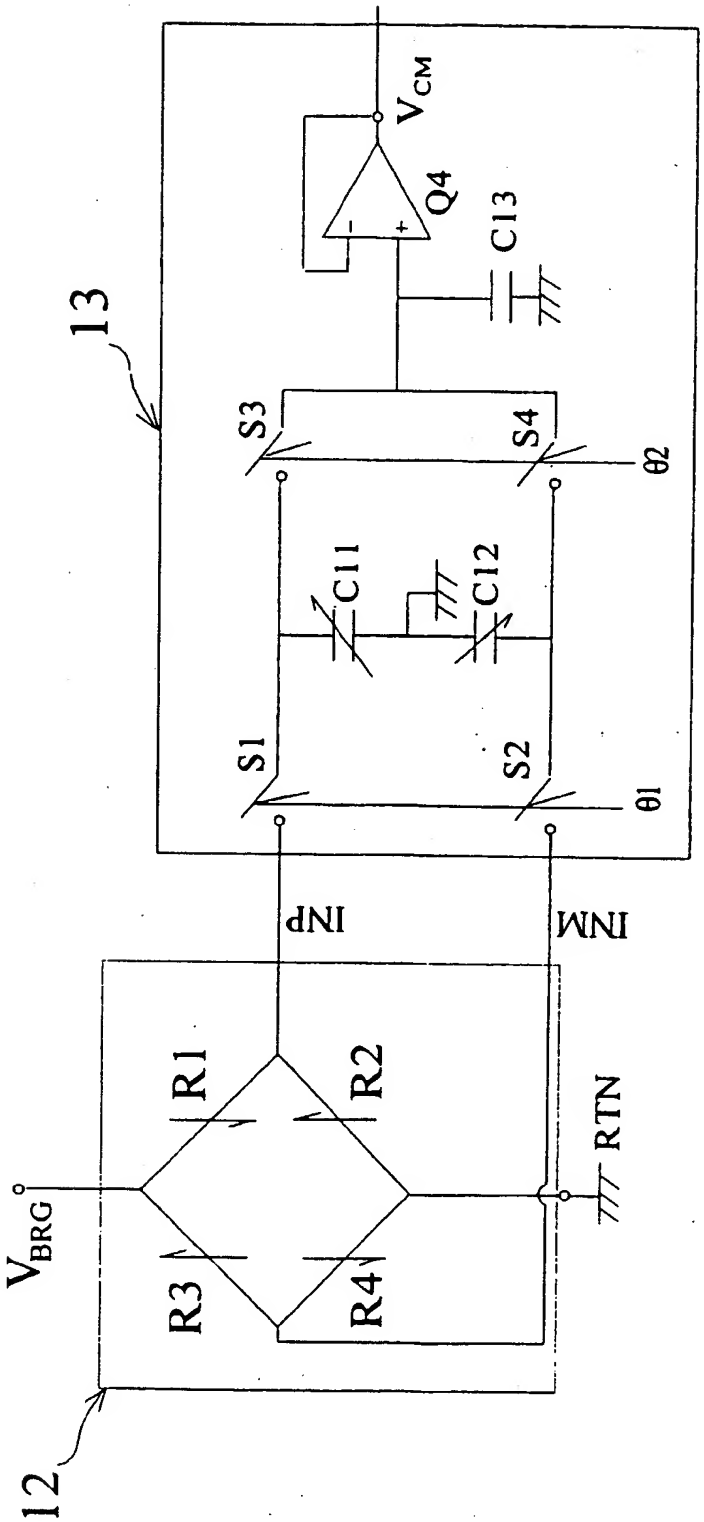
13
V_{CM}
Q4
C13
S3
S4
θ2
C11
C12
S1
S2
θ1
INP
INM
R1
R2
R3
R4
RTN
V_{BRG}
12

Fig 2b

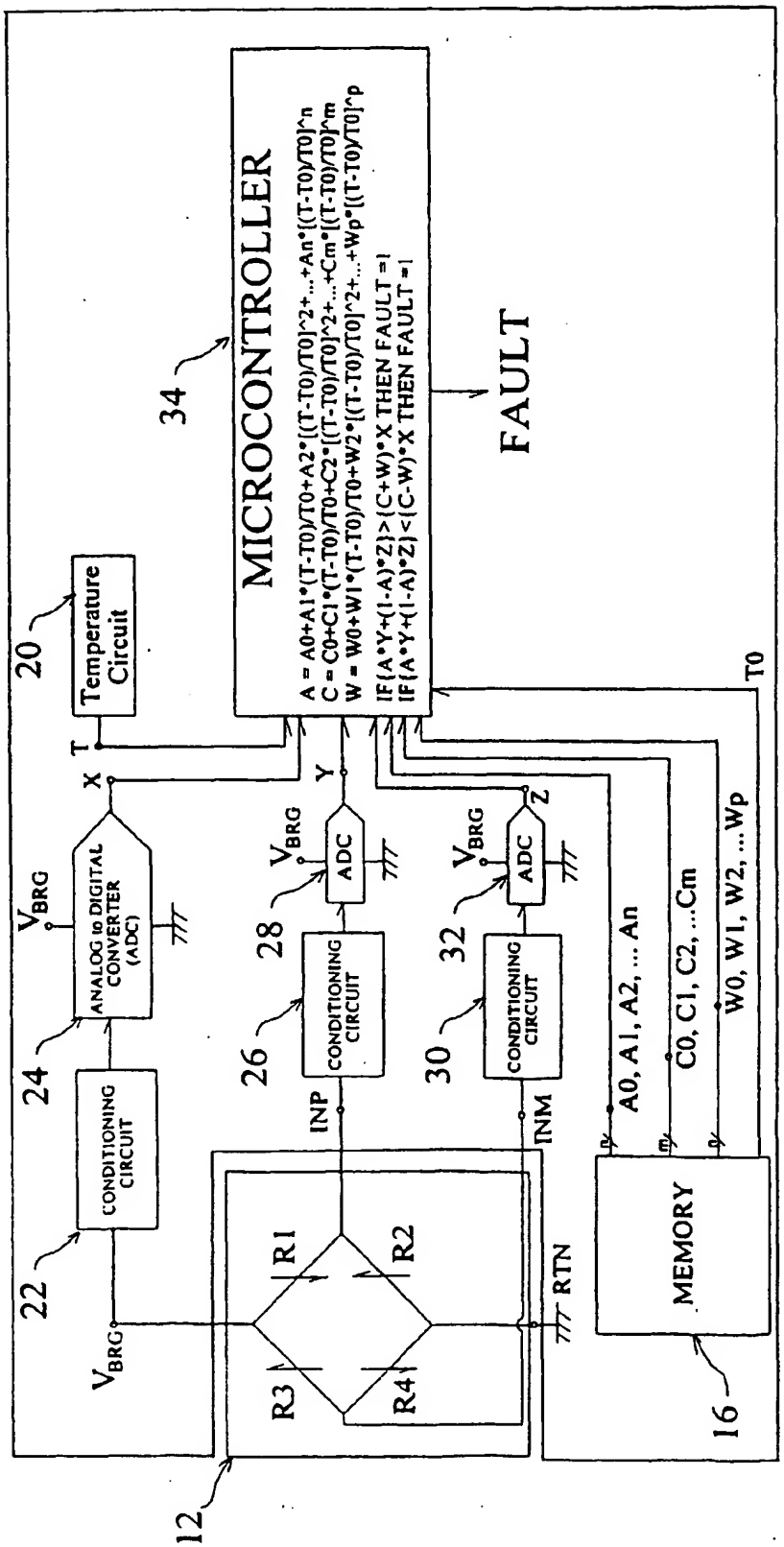
MICROCONTROLLER
A = A0+A1*(T-T0)/T0+A2*[(T-T0)/T0]^2+...+An*[(T-T0)/T0]^n
C = C0+C1*(T-T0)/T0+C2*[(T-T0)/T0]^2+...+Cm*[(T-T0)/T0]^m
W = W0+W1*(T-T0)/T0+W2*[(T-T0)/T0]^2+...+Wp*[(T-T0)/T0]^p
IF{A*Y+(1-A)*Z}>{C+W)*X THEN FAULT=1
IF{A*Y+(1-A)*Z}<(C-W)*X THEN FAULT=1
FAULT
34
Temperature Circuit
20
T
X
Y
Z
T0
ANALOG to DIGITAL CONVERTER (ADC)
ADC
ADC
CONDITIONING CIRCUIT
CONDITIONING CIRCUIT
CONDITIONING CIRCUIT
24
26
28
30
32
22
INP
INM
RTN
R1
R2
R3
R4
VBRG
VBRG
VBRG
VBRG
MEMORY
16
A0, A1, A2, ... An
C0, C1, C2, ...Cm
W0, W1, W2, ...Wp
12

Fig 2c

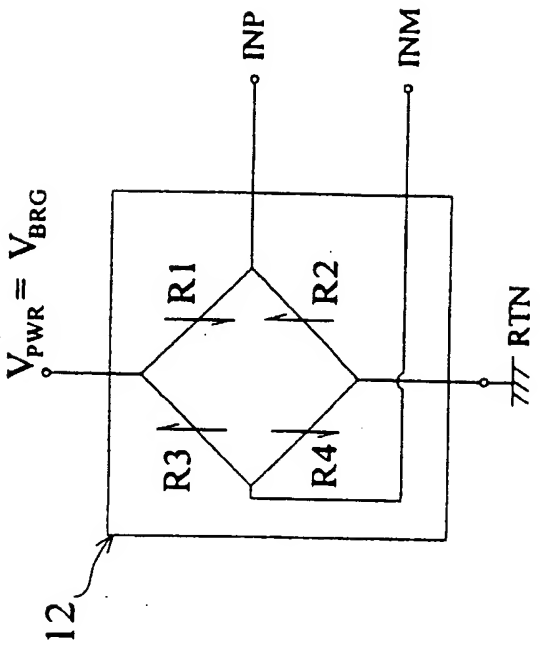

Fig 3

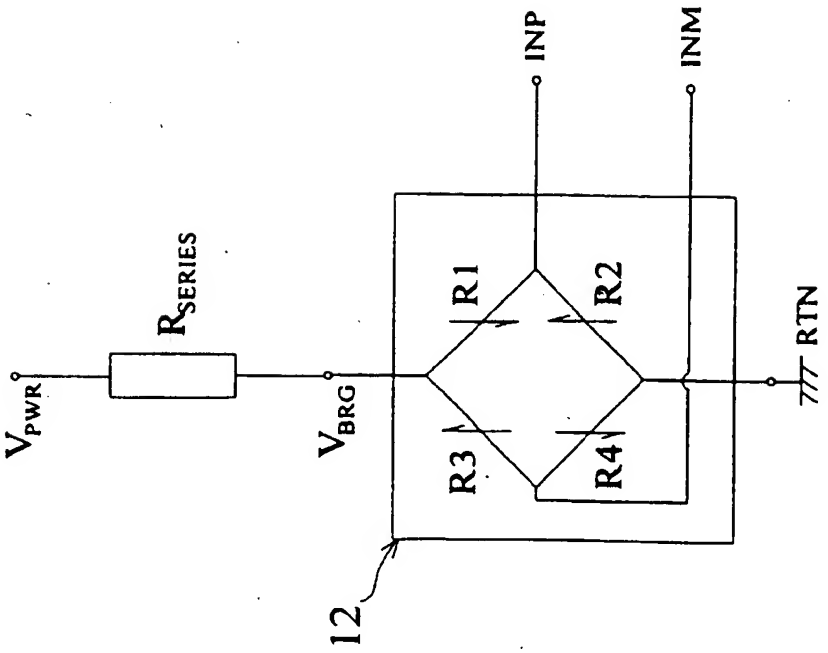

Fig 3a

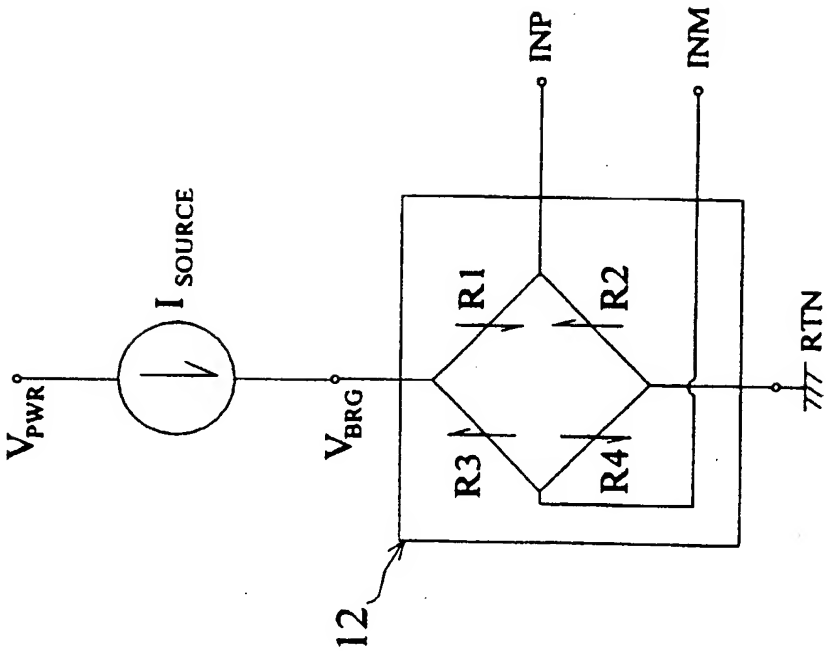

Fig 3b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 31 1374

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G01D

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 March 2001	Lut, K

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